

Meet our Team @ the booth:

Paweł Banachowicz

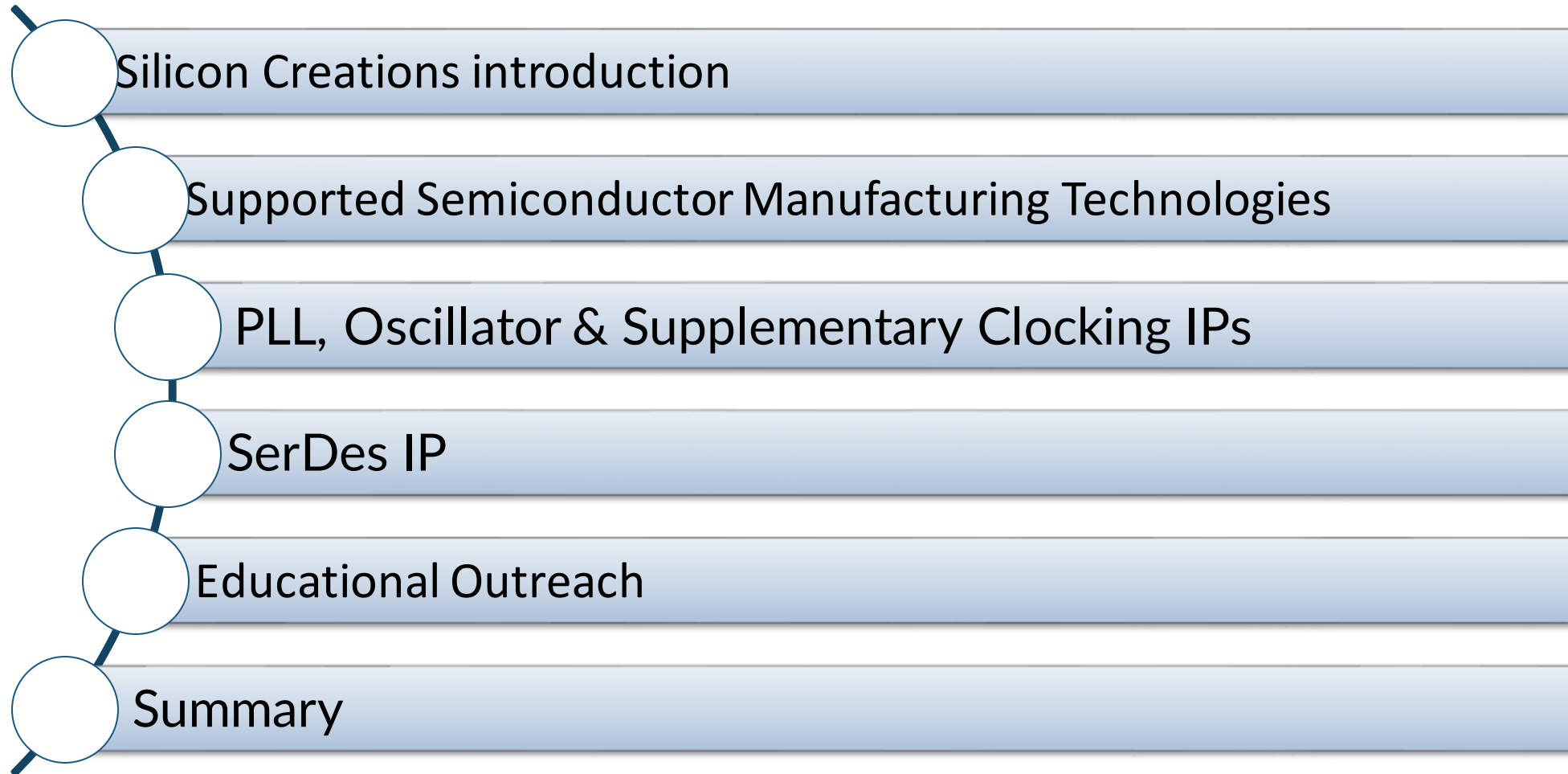
Director of Analog/Mixed-Signal Design

Krzysztof Kasiński

Director of IP Verification & Validation Laboratory

Joanna Iwanicka

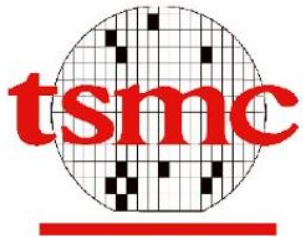
IP Verification & Validation Engineer



- IP provider of **PLLs, Oscillators** and **High-speed Interfaces**
- Founded 2006 – self-funded, profitable and growing
- High quality development, award winning support
- Design offices in **Atlanta, USA** and **Krakow, Poland**
- >400 customers

Mass production in all FinFET nodes down to 5nm with 3nm PLLs silicon-proven





TSMC Open Innovation Platform®
IP & 3DFabric™ Alliance

Samsung Advanced Foundry Ecosystem (SAFE™)
IP Partner Program

Intel Foundry Services
Accelerator IP Alliance



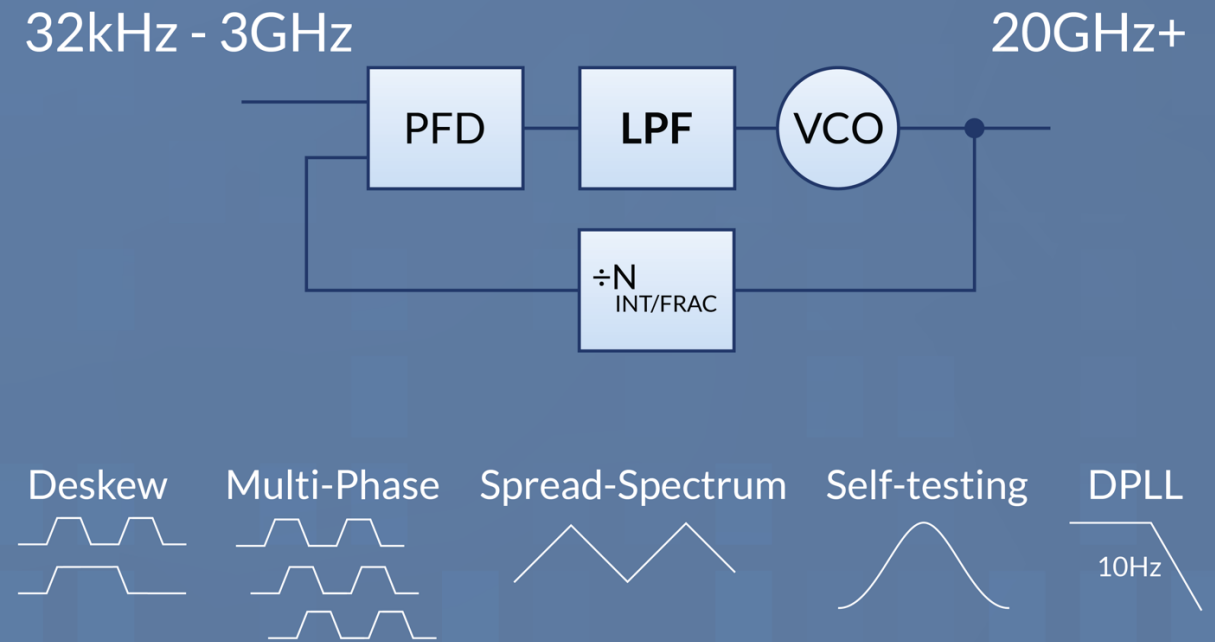
TSMC Mixed Signal Partner of the Year
2017,2018,2019,2020,2021,2022

Highest volume analog IPs
Our **PLLs** are on **+10M TSMC wfrs**
Robust design and good QA (ISO9001)

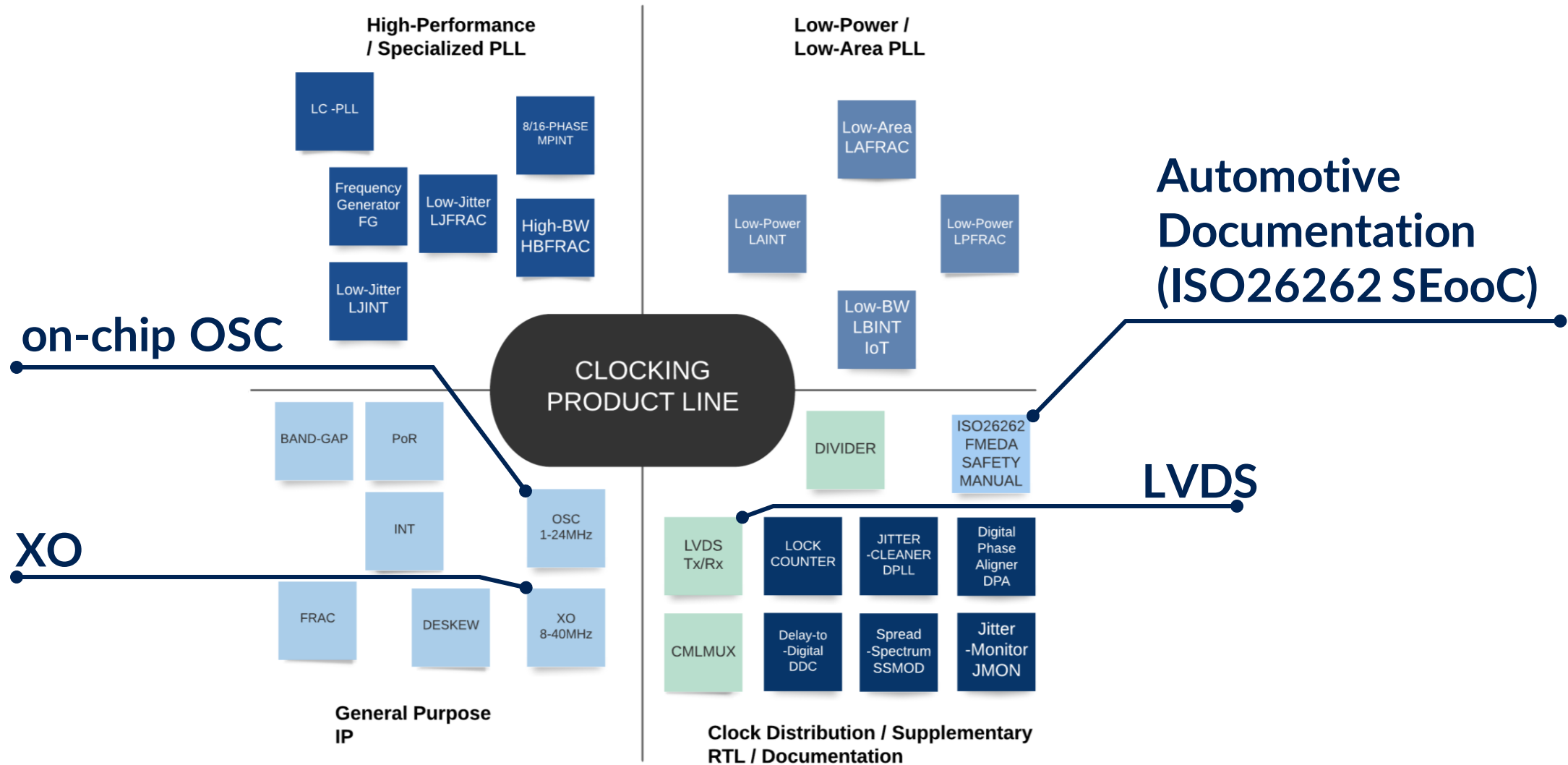
PLL products include
General purpose Integer & Fractional,
application specific options:
Low-Jitter, μ W IoT, Automotive, Low Area, Low-Power
Available in **3nm-180nm**

PLLs & Oscillators

Power | Jitter | Area Optimized

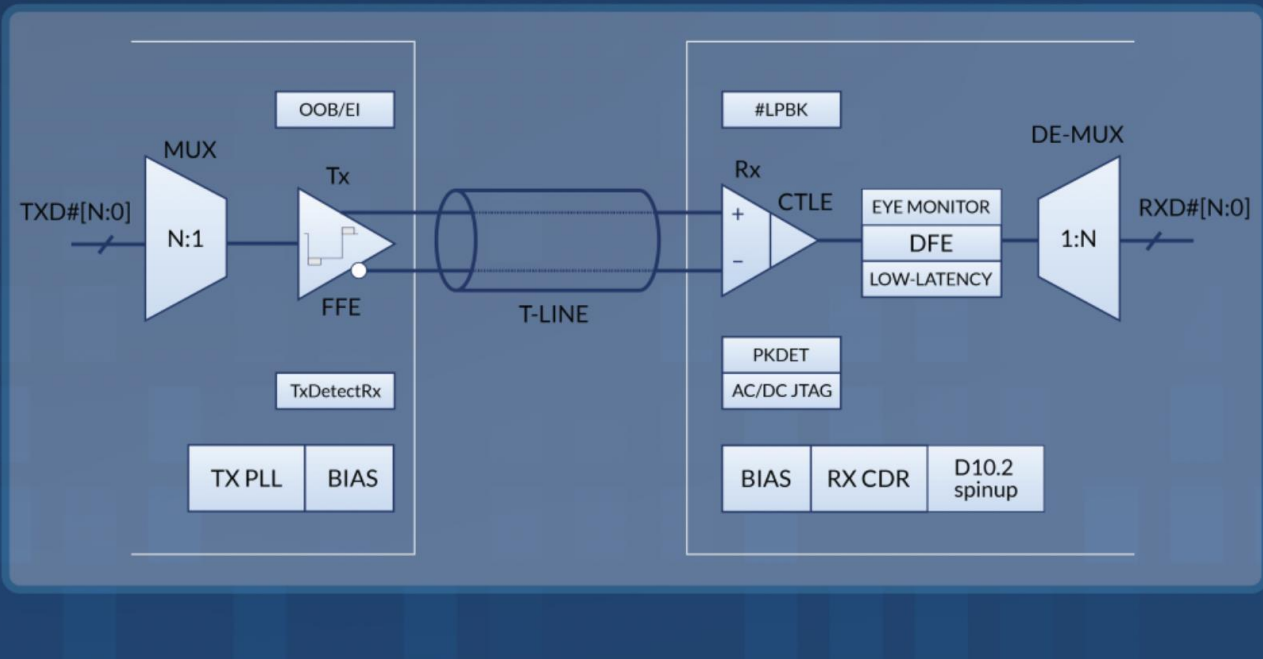


PLLs and supporting Hard-Macro & RTL IPs



Multiprotocol NRZ SerDes

PCIe, Display Port, Ethernet, USB 3.x & more | Low-latency



- Ultra-Low Power
- 14-tap/5-tap DFE architectures
- Other interfaces: LVDS,CML

FinFET MP SerDes PMA eye-diagram:

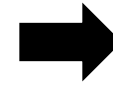


- Kraków & Atlanta
- 16 full testbenches
- PLL, OSC & SERDES targeted
- Silicon-proven IPs



Chip Companies
IP Companies
Semiconductor Industry
Universities
Schools

& Young People
Interested in electronics



Later pursuing education & career in
Microelectronics, Electronics, Photonics,
Power Electronics, Device Research

...

Silicon Creations Educational Outreach



Silicon Creations Educational Outreach

Early education (visitors, lectures, games) Technical High-Schools & Universities (visitors, lectures, interns, contests)



**4-DAY COURSE ON
MICROELECTRONICS
BY PROF. MICHIEL STEYAERT**

Prof. Michiel Steyaert
(KU Leuven, Belgium)



IEEE Solid-State Circuits Society Chapter Poland



MTM Mikroelektronika w Technice i Medycynie

274 obserwujący • 7 obserwowanych



IEEE Solid-State Circuits Society
Chapter Poland Technical Meeting

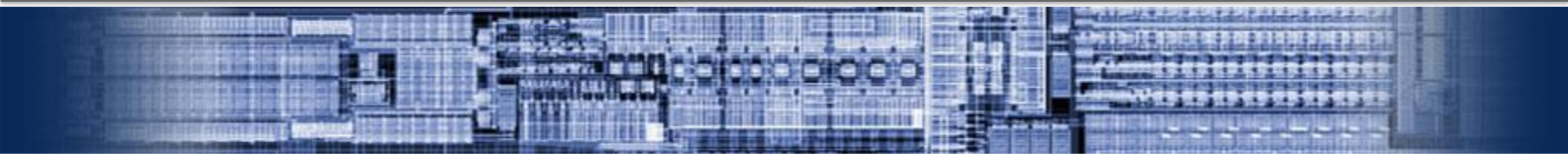
**Nanoscale FinFET Technology for
Circuit Designers**

Dr. Alvin Lake (NXP)



IEEE SSCS Chapter Poland Lecturers: Willy Sansen, Michiel Steyaert, Bogdan Staszewski & others (including Silicon Creations employees)

Result: **75%** of Silicon Creations employees graduated from MTM Microelectronics (AGH University) course.



Thank You For Your Attention!

- For more information about IP, please contact sales@siliconcr.com
- For careers in Poland, please contact hrpl@siliconcr.com
- Meet our Team at the **booth**
- Listen to technical talk this Thursday (Sesja Wykładowa II) 10.20 - 10.35
Testowanie systemów generacji zegara w nowoczesnych mikroukładach typu SoC
Krzysztof Kasinski, Joanna Iwanicka, Magdalena Chrobak

Paweł Banachowicz
Director of Analog/Mixed-Signal Design

Krzysztof Kasiński
Director of IP Verification & Validation Laboratory

Joanna Iwanicka
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