

# **ELTE Conference 2023 in Poland**

## **Exploring Wide Bandgap Semiconductor Research Collaboration Opportunities in Poland**

**Dr. Robert Chau**

**Intel Senior Fellow, Intel Technology Development**

**Director of Intel Europe Research**

**IEEE Fellow, Member of U.S. National Academy of Engineering**

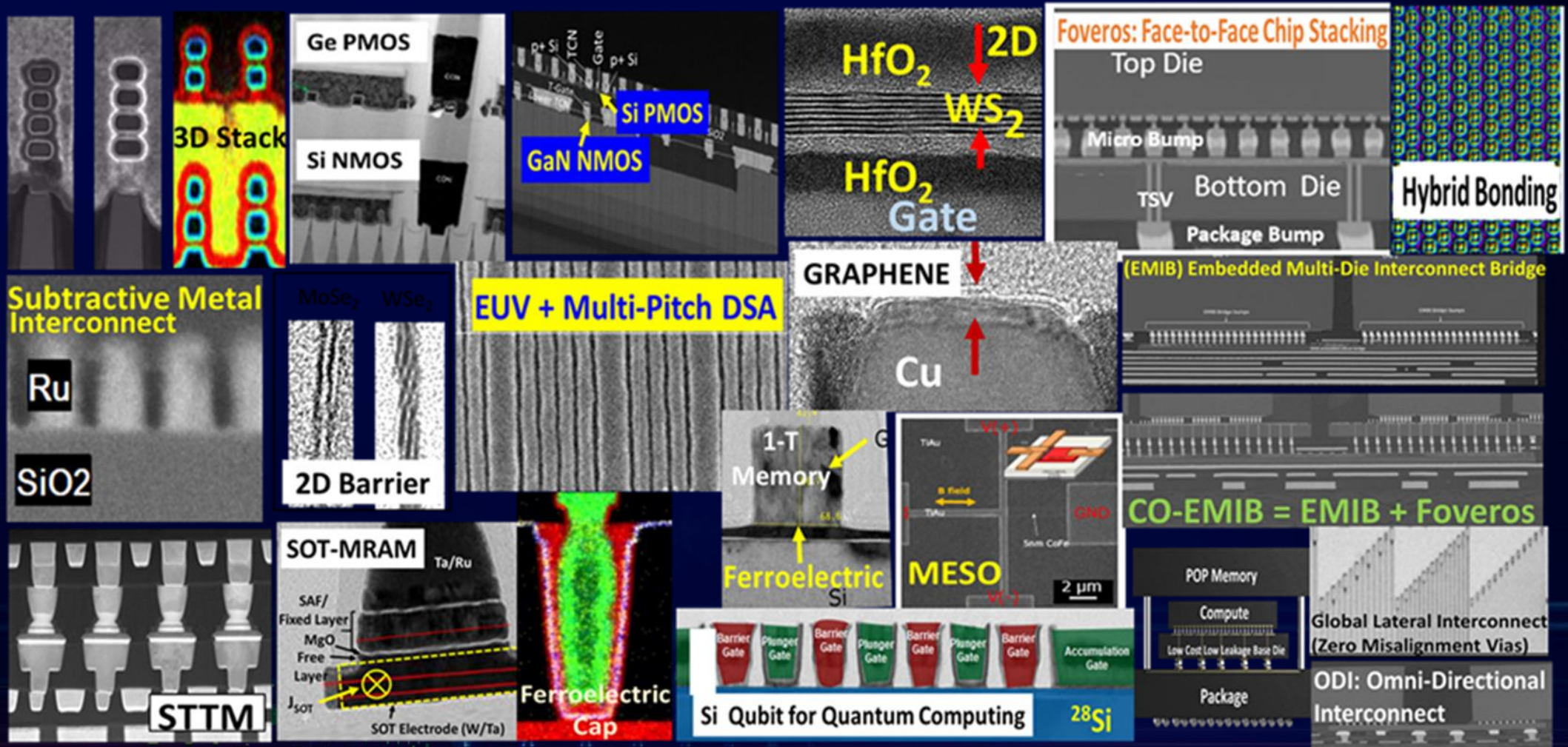
**April 19, 2023**

# Robert Chau, Director of Intel Europe Research

- 35 years with Intel.
- Intel Senior Fellow since 2005.
- General Manager of Intel Components Research organization 2014-2022.
- Director of Intel Europe Research 2022 - present (**relocated from U.S. to Brussels in 2022**).
- 2012 IEEE Jun-ichi Nishizawa Medal for Strained-Si and High-k/Metal-Gate technologies.
- 2015 Intel Inventor of the Year Award for Intel's FinFET technology.
- Holds >480 U.S. patents.
- IEEE Fellow.
- Elected Member, U.S. National Academy of Engineering.

# Microelectronics Advancement Requires Semiconductor and Packaging R&D

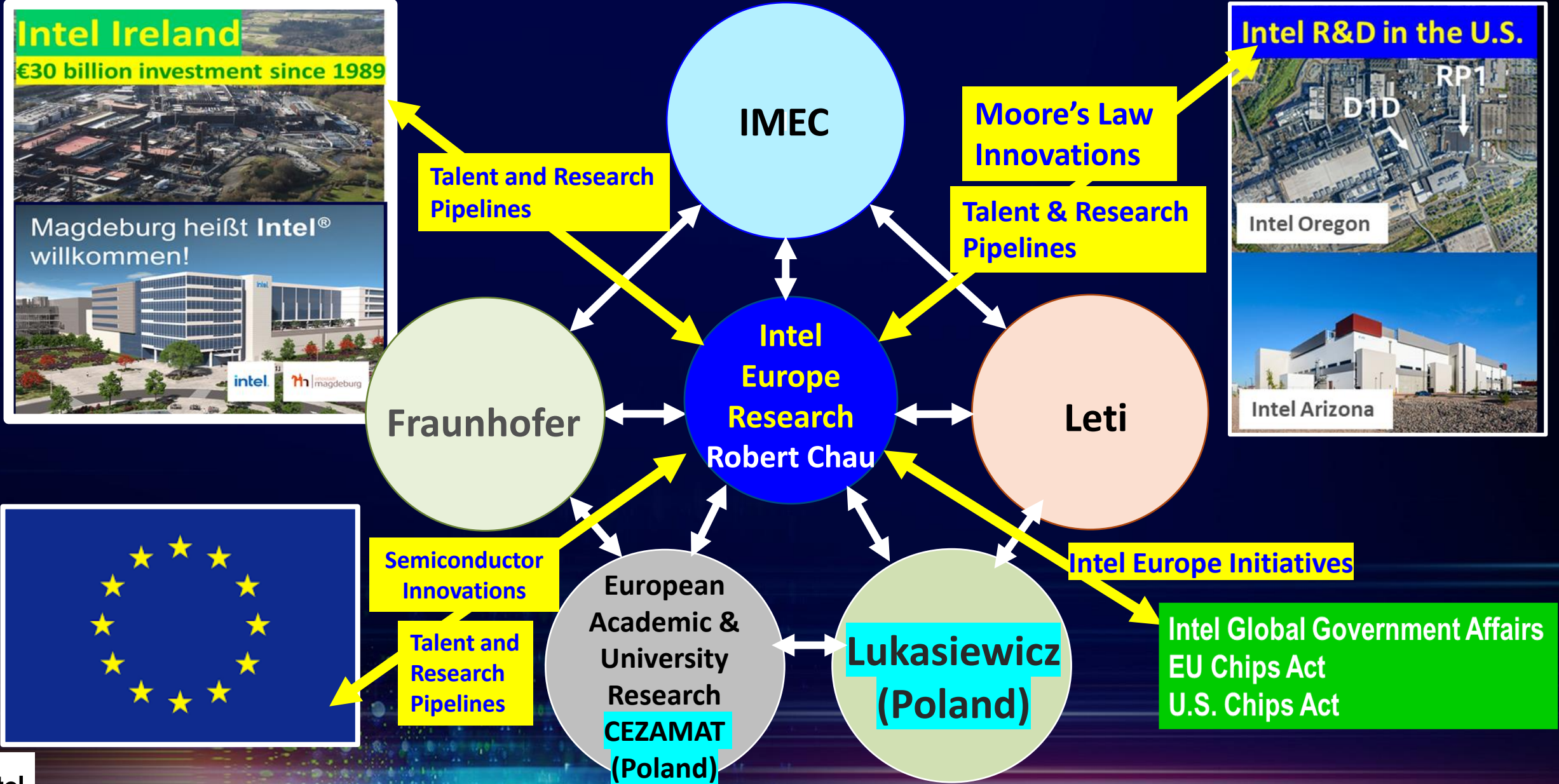
## Moore's Law Scaling + New Functions



Transistor, Interconnect, Patterning, Memory, Packaging, 3D Integration, New Materials, New Functions

Source: Robert Chau, Intel, IEDM 2019 Keynote

**Intel Europe Research (Robert Chau): Intel-European RTOs R&D collaborations in 1) accelerating semiconductor process and packaging R&D advancement in Europe and 2) driving Moore's Law and beyond.**



# Intel Europe Research and Poland RTOs

- Intel established its presence in Poland 24 years ago.
- Intel has established a large software R&D center in Gdansk with ~2400 employees.
- Intel Europe Research (Robert Chau) visited CEZAMAT in Oct 2022 and gave keynote speech at the 2022/2023 academic year inauguration:



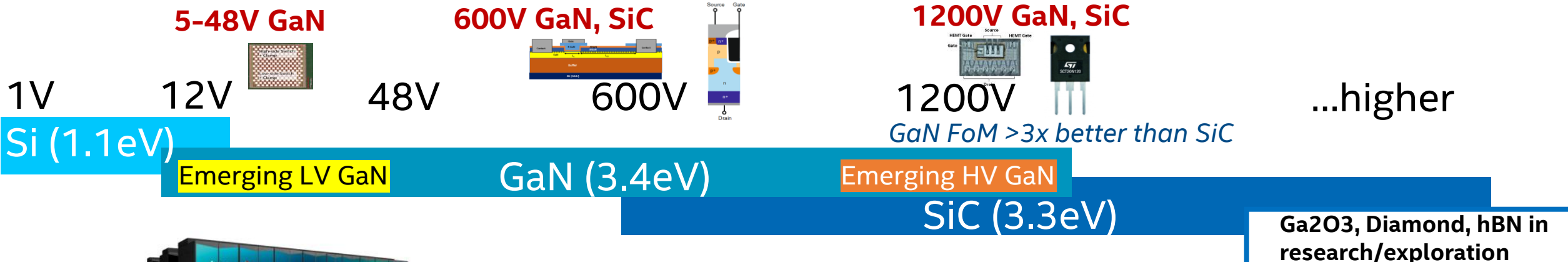
- Piotr Dardzinski (former Lukasiewicz president) and Robert Chau (Intel) met in Brussels Nov 2022 to discuss R&D landscapes in Poland and Intel-Lukasiewicz research collaboration opportunities.
- Intel's Robert Chau and IMEC's Luc Van den hove (CEO) co-hosted Lukasiewicz at IMEC Leuven in Feb 2023 to discuss joint Intel/Lukasiewicz/IMEC research collaboration opportunities.
- Lukasiewicz (Jakub Kaczmarek) and Intel (Robert Chau) are organizing a joint technical workshop in Poland in 2023 on wide bandgap semiconductors R&D (contact: Jakub Kaczmarek @Lukasiewicz)
  - ❖ To stimulate discussions on wide bandgap semiconductors and explore joint R&D opportunities

# Wide Bandgap Semiconductors for RF and Power Applications

	Ge	Si	SiC	GaN (AlGaN)	Diamond	hBN
E <sub>g</sub> (eV)	0.67	1.1	3.26	3.39	5.45	6.4
electron mobility (cm <sup>2</sup> /Vs)	3900	1350	700	1900	1900	200
hole mobility (cm <sup>2</sup> /Vs)	1900	450	20	20	2000	?
electron charge density (e <sup>20</sup> cm <sup>-2</sup> )	>10	>10	0.5	5	~1	?
v <sub>peak</sub> (10 <sup>7</sup> cm/s)	1	0.7	2	2.5	2.7	?
E <sub>Critical</sub> (MV/cm)	0.15	0.3	3	3.3	5.6	15
Thermal conductivity (W/cm K)	0.6	1.5	3.3-4.5	2	20	21
<b>RF Johnson's FOM = E<sub>Critical</sub> * v<sub>peak</sub></b>	0.7	1.0	<b>29</b>	<b>39</b>	<b>72</b>	?
<b>Power Baliga's FOM = μ<sub>n</sub> * E<sub>Critical</sub><sup>3</sup></b>	0.5	1.0	<b>443</b>	<b>1441</b>	<b>4460</b>	<b>5698</b>

SiC most mature; GaN higher performance (higher mobility, higher charge density and higher FOMs) than SiC but requires more R&D; Diamond and hBN in research/exploration phase

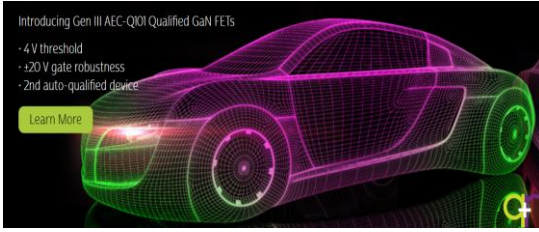
# Wide Bandgap Semiconductor Opportunities



**Datacenter**



**Fast Chargers**



**Automotive**



**Defense, Space**



**Aerospace**

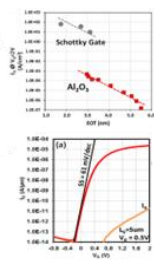
- RF Base Station
- 5G/6G Small Cells
- Mobile Handsets

- SiC most mature and dominates at >1000V (but lower performance than GaN)
- GaN opportunities in < ~600V (higher performance than SiC) but requires more R&D.
- More discussions at the upcoming 2023 Lukasiewicz-Intel technical WS in Poland (contact: Jakub Kaczmarek @Lukasiewicz)

# Intel's GaN research has been focusing on low-voltage (5-48V) applications and large-wafer processing

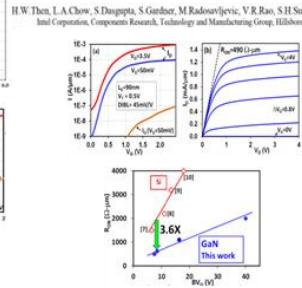
IEDM 2013

Experimental Observation and Physics of "Negative" Capacitance and Steeper than 4th-Voltade Subthreshold Swing in AlkxGa<sub>1-x</sub>N/AlN/GaN MOS-HEMT on SiC Substrate



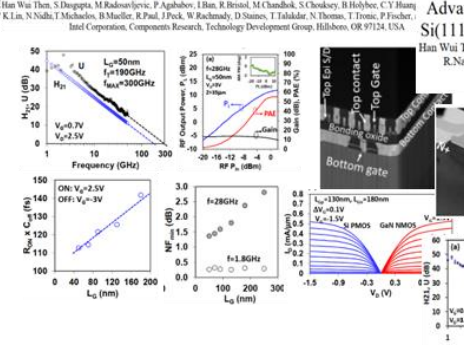
VLSI 2015

High-Performance Low-Leakage Enhancement-Mode High-K Dielectric GaN MOS-HEMTs for Energy-Efficient, Compact Voltage Regulators and RF PAs for Low-Power Mobile SoCs



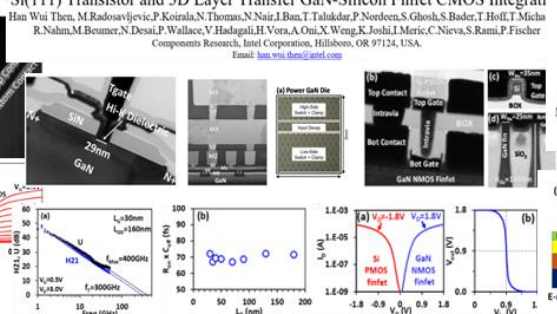
IEDM 2019

3D heterogeneous integration of high performance high-K metal gate GaN NMOS and Si PMOS transistors on 300mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5G and beyond) and SoC applications



IEDM 2021

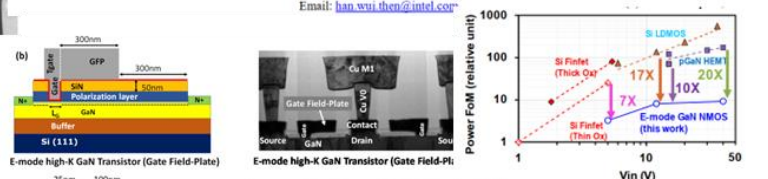
Advanced Scaling of Enhancement Mode High-K Gallium Nitride-on-300mm-Si(111) Transistor and 3D Layer Transfer GaN-Silicon FinFet CMOS Integrati



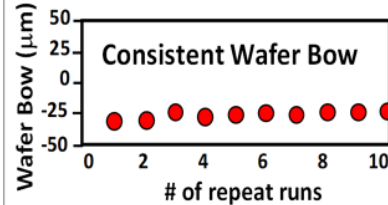
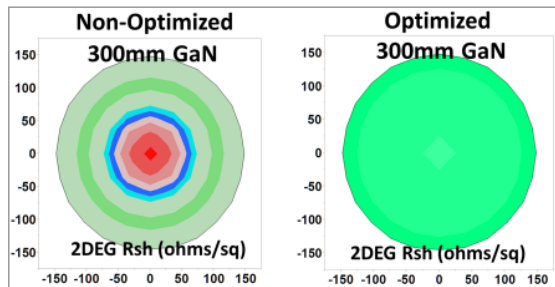
IEDM 2022

Scaled Submicron Field-Plated Enhancement Mode High-K Gallium Nitride Transistors on 300mm Si(111) Wafer with Power FoM ( $R_{ON}Q_{GG}$ ) of 3.1 mohm-nC at 40V and  $f_T/f_{MAX}$  of 130/680GHz

Han Wui Then, M. Radosavljevic, P. Koirala, M. Beumer, S. Bader, A. Zubair, T. Hoff, R. Jordan, T. Michaelos, J. Peck, I. Ban, N. Nair, H. Vora, K. Joshi, I. Meric, A. Oni, N. Desai, H. Krishnamurthy, K. Ravichandran, J. Yu, S. Besch, D. Frolow, A. Hubert, A. Latorre-rey, S. Rami, J. Rangaswamy, Q. Yu, P. Fischer



## MOCVD-Grown GaN on 300mm Silicon (111)



### A Manufacturable 300mm GaN Process on Si (111)

- Uniform 2DEG and Crystal Quality
- Consistent Wafer Bow

Source: Robert Chau, Intel, IEDM 2019 Keynote  
Han Wui Then, Intel, IEDM 2019, 2021, 2022



# Closing Remarks

- **Strong research collaborations between Intel Europe Research, Poland's RTOs (Lukasiewicz, CEZAMAT) and Polish universities will accelerate semiconductor R&D advancement in Poland and Europe.**
- **Joint Lukasiewicz-Intel 2023 technical workshop in Poland on wide band-gap semiconductors R&D (contact: Jakub Kaczmarek @Lukasiewicz)**

